IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Craig T. Salling, et al. Art Unit: TBD

Serial No.: 10/051,639 Examiner: TBD

Filed: 01/18/02 Docket: TI-32536

For: ESD Improvement by a Vertical Bipolar Transistor with Low Breakdown Voltage and High Beta

LETTER TO THE OFFICIAL DRAFTSPERSON

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service on 3-27-02 as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Karen Vertz 3-27-02
Karen Vertz Date

Assistant Commissioner for
Patents
Washington, D. C. 20231

Dear Sir:

Enclosed are **TWO (2)** sheets of formal drawings for the above-referenced case. Please charge any necessary fees to Deposit Account No. 20-0668 of Texas Instruments Incorporated. This sheet is enclosed in triplicate.

Respectfully submitted,

Gary C. Honeycutt

Gary C. Honeycutt
Reg. No. 20,250
Attorney for Applicants

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(214) 939-8651

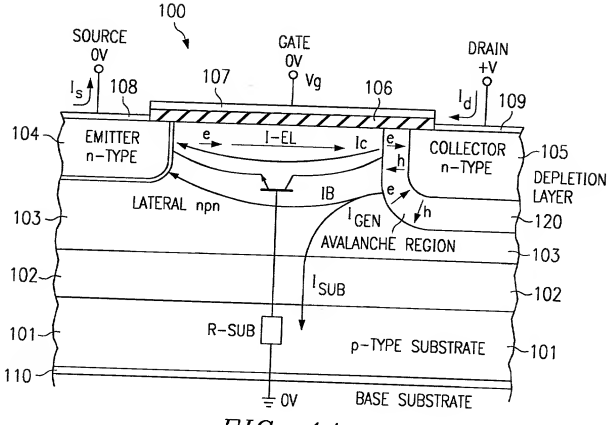

FIG. 1A
(PRIOR ART)

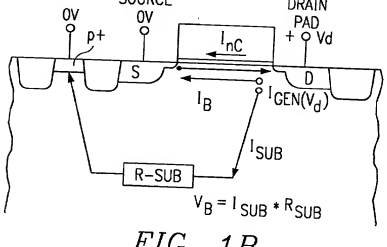

FIG. 1B
(PRIOR ART)

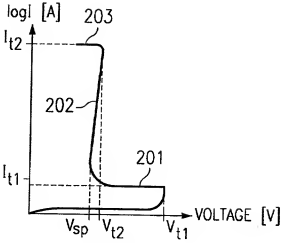

FIG. 2
(PRIOR ART)

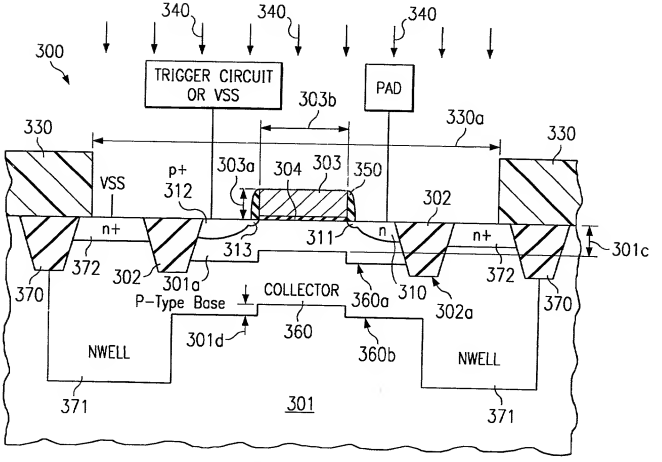

FIG. 3